NAME

EGR/CS 433(430)
Advanced Computer Engineering (Parallel Processing) LECTURE & LAB

FINAL EXAM

J. Wunderlich, PhD

This is a closed-book, closed-notes, no-calculators exam. Write all answers on blank paper supplied to you. Write your name at the top of every page.

PARTIAL TAKE-HOME EXAM: this exam is given to you the week before the in-person final, but you can't bring any written answers to the actual exam; i'll give you another copy of this exam, with the blanks filled in, for the actual exam

1. (25 points total) HARDWARE vs. SOFTWARE PARALLELISM, GRAIN PACKING & SCHEDULING

Given the following equations of scalar variables: _____

A. (7 points) Graph instructions (in circles) and arrows indicating flow of execution, for a SOFTWARE (IDEAL) implementation, AND calculate the **AVERAGE PARALLELISM** = (# of instructions) / (# of cycles)

B. (7 points) Graph instructions (in circles) and arrows indicating flow of execution, for a __-WAY SUPERSCALAR PROCESSOR HARDWARE implementation, AND calculate the **AVERAGE PARALLELISM** = (# of instructions) / (# of cycles). ASSUME:
- __ memory accesses ("load" or "store") can be done simultaneously
- __ arithmetic instruction can be done at a time **in this one core/processor**
- You must use STORE instructions in the last cycle(s) of your execution

C. (7 points) Graph instructions (in circles) and arrows indicating flow of execution, for __ CORE SMP HARDWARE (communicating through "Loads" & "Stores"), AND calculate the **AVERAGE PARALLELISM** = (# of instructions) / (# of cycles). ASSUME:
- __ memory accesses ("load" or "store") can be done simultaneously
- __ arithmetic instruction can be done at a time **on each core/processor**
- You must use STORE instructions in the last cycle(s) of your execution

(4 points) Describe in words & pictures **GRAIN PACKING** to optimize **SCHEDULING**. Pick or create any example you wish.

2. (12 points total) PARALLEL PROCESSING INTERCONNECT ARCHITECTURES

A. (8 points total) For a _____ topology (**STATIC** interconnect architecture) with _____ interconnection links, calculate:
   i. (2 points) Network "Diameter"
   ii. (2 points) Node "Degree"
   iii. (2 points) Network "Bisection Width"
   iv. (2 points) The total number of physical wires through the Network Bisection

B. (4 points) Sketch the _____and_____ **DYNAMIC** interconnect architectures and explain why one is more scalable than the other

3. (25 points total) CACHE DESIGN

For a _____ **Main Memory** that has byte addressing, and a cache that holds _____ of _____ **blocks**:
   a. (5 points) Sketch and label Main Memory including addresses in HEX
   b. (**20 points**) For a _____ **MAPPED** cache:
      i. Sketch and label the cache including cache-lines (for the cache blocks) in HEX
      ii. Show the calculation of the cache tag size
      iii. Re-sketch and label Main Memory to show how it is organized ("chunked") into groups because of the size of the tag
      iv. State both the hit and miss operation including a cache-miss replacement policy

4. (21 points) SCALABILITY IN PARALLELL PROCESSING

Summarize with one paragraph each, and sketches as needed, the scalability aspects in all **seven** subtopics listed and discussed in our lecture on scalability in **HIGH PERFORMANCE COMPUTING (HPC)**, posted on YouTube: https://www.youtube.com/watch?v=hlcS4PwgtMM plus other lectures, and custom lab manuals on the Sixth and seventh subtopics (i.e., "#6 FPGA's, and "#7 IBM").

5. (17 points) Write an essay about <u>only one</u> of the following:

NEURAL NETWORK PROCESSOR DESIGN
including discussion of:

A. In a sentence or two, compare and contrast the two Neurocomputers developed by Dr W in the early 1990's, in his draft book chapter
B. Draw and label graphs of three Neuron Transfer functions, including the Rectified Linear Unit in the 2018 paper we discussed
   - *"Deep Learning using Rectified Linear Units (ReLU)" by A. Agarap* – Neural Network Transfer Function Hardware
C. Explain Dr W's Transfer function implementation in his **single-chip parallel processing Neurocomputer with on-chip learning**
D. Explain how you believe the **"Fontons"** in the 2017 supercomputer paper we discussed could be used for neurocomputations
   - *"Simultac Fonton: A Fine-Grain Architecture for Extreme Performance beyond Moore's Law" by M. Brodowicz and T. Sterling*

E. With words and sketches, describe your neural network hardware in your last major laboratory project

- **Neurocomputer Reference material** from my *EGR434 Robotics & Machine Intelligence* course
  - Wunderlich, J.T. (2004). **Top-down vs. bottom-up neurocomputer design.** In *Intelligent Engineering Systems through Artificial Neural Networks, Proceedings of ANNIE 2004 Int'l Conference, St. Louis, MO.* H. Dagli (Ed.): Vol. 14. (pp. 855-866). ASME Press. [Paper Award]
  - Wunderlich Deep Learning Book Chapter Draft & Neural Network Processor Designs PPTX-w/audio PDF MP4 YouTube
  - Wunderlich Machine Intelligence History -- Draft book chapter PPTX-w/audio PDF MP4 YouTube
  - Calculus for Machine Learning PPTX-w/audio PDF MP4 YouTube
  - Machine Intelligence Intro -- Symbolic AI vs Neural Networks PPTX-w/audio PDF MP4 YouTube
  - Neural Network Code MP4 YouTube

OR:

IBM S/390 & Z-Series PARALLEL PROCESSOING (supercomputers)

J. Wunderlich Ph.D. Advisory Level Engineer & Researcher **MP4 YouTube**

including discussion of:

A. Machine Evolution PDF PPTX
B. Processor Design including early Cache and Out-of-order Execution Design PDF
C. Principles of Operation ("POPs") PDF
D. Quick Reference PDF
E. **BRANCH PREDICTION** with Branch History Table **(BHT)** – to *cache* branch addresses PDF
F. **VIRTUAL ADDRESS PREDICTION** with Translation Lookaside Buffer **(TLB)** - to *cache* Virtual Address Translations PDF
G. **QUALITY CONTROL / VERIFICATION** with Wunderlich "Controlled Randomness" *patented by IBM* PDF PPT
   Wunderlich, J.T. (2003). **Functional verification of SMP, MPP, and vector-register supercomputers through controlled randomness.** In *Proceedings of IEEE SoutheastCon, Ocho Rios, Jamaica,* M. Curtis (Ed.): (pp. 117-122). IEEE Press. PPTX-w/audio PDF MP4 YouTube

   including discussion of:
   - What does IID (Independent and Identically Distributed) mean in reference to Random Number Generators
   - What is a three-tuple graph in assessing the quality of a Random Number Generator (describe a bad one)
   - Discuss how Dr W's research of combining seven random number generators, and his developing API's for the IBM supercomputer test-kernel, provided varying options for the systems level programmers at IBM (be specific)
   - List the three environments that the IBM supercomputer test-kernel ran in
   - Why did the selected Random Number Generators need to be run in reverse